10Gb/s Clock Extraction and Data Regeneration Circuit Implemented with Phase-Locked Loop

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ABSTRACT

A PLL clock-extraction and data-regeneration circuit(CEDAR) for 10Gb/s optical transmission system was realized in a hybrid IC form. The jitter characteristics satisfied the recommendations of ITU-T. The CEDAR compensated against the temperature was tested for the temperature from -10 °C to 60 °C and showed no increase of error.

INTRODUCTION

The transmission rate of the optical communication has been drastically increased since it was introduced in the late 1970s. At the present time, 10Gb/s systems are being deployed for the commercial service. The high-speed circuit blocks for the 10Gb/s signal processing, however, are still remained to be improved for the higher operating margin and the higher reliability. Especially, the clock-extraction and data-regeneration circuit (CEDAR) which has been implemented with a dielectric resonator should be improved to maintain a sufficient decision phase margin over a wide operating temperature.

The function of CEDAR is to extract the clock from the transmitted data and retime the data with the extracted clock. The transmitted data includes much timing jitter which is generated from the chromatic dispersion and the noise of optical transmission channel. The CEDAR should be designed to be tolerable to this timing jitter and generate a clock with a small timing jitter. The narrow band-pass filter for 10GHz clock extraction in CEDAR can be realized with either a dielectric resonator filter or a phase-locked loop(PLL) filter. The PLL has an advantage that the center frequency of the filter always coincides with the clock frequency. There was a report on the 10Gb/s PLL CEDAR and it, however, showed only the possibility of the monolithic IC for 10Gb/s PLL CEDAR[1]. In this work, we developed a PLL CEDAR in a hybrid IC format, and fully characterized and successfully adopted it for 10Gb/s optical transmission for the first time.

CIRCUIT CONFIGURATION

Fig. 1 shows the block diagram of CEDAR consisting of an input buffer, a clock extraction circuit, 2 sets of phase shifter, and a decision circuit. The 10Gb/s data amplified by the input buffer is fed both to the decision circuit and to the clock extraction circuit. The clock extraction circuit extracts the clock from the 10Gb/s NRZ data. The extracted clock is connected to the decision circuit through a phase shifter. The phase shifter is to adjust the clock phase to an optimum position for the decision of the incoming data. The phase shifter was a reflection-type analog phase shifter implemented with 4 varactor diodes, and a 90-degree hybrid coupler. The total phase shift was 380 degrees and the insertion loss was -4.5 ± 0.8 dB with the control voltage varied from 0 to 15V.

The performance of CEDAR largely depends on the clock extraction circuit. Fig. 2 shows the block diagram of the clock extraction circuit consisting of a NRZ-to-PRZ converter and a PLL filter. The NRZ-to-PRZ converts the 10Gb/s NRZ data into a PRZ format, in which a discrete clock signal of 10GHz are included along with the noise

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generated from the randomness of the data[2]. The clock is obtained after filtering out the noise around the clock signal with a band-pass filter of 0.9GHz 3dB bandwidth. The PLL circuit performed as a narrow band-pass filter was realized in a quadri-correlator frequency- and phase-locked loop[3,4]. The dc signal at the output of the IF mixer in Fig. 2 is proportional to the frequency difference between the clock and the VCO, and is negatively fed back to the VCO reducing the frequency difference. This dc signal, however, causes a large voltage offset in PLL after the FLL completes its function. A switching circuit was built into the conventional FPLL to switch off the FLL signal and avoid the large voltage offset originated from the FLL signal.

Fig. 3 shows the photograph of the CEDAR. It consists of 4 alumina substrates of 25 mil thick, 2 sets of 10GHz mixers, and a FPLL loop filter built on a printed circuit board. The circuit size was 99.4 x 95.2 x 15.3 mm^3.

PERFORMANCE

The CEDAR is evaluated by jitter tolerance, jitter transfer, jitter generation, and phase margin. Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter causing a 1dB power penalty. A sinusoidal jitter is inserted into 10Gb/s data by modulating the frequency of the reference clock of the pulse pattern generator(PPG) with a sinusoidal wave. Fig. 4 shows jitter tolerance measured at jitter frequencies ranged from 50 kHz to 50 MHz. The measured jitter tolerance shown in solid circles is larger than the jitter tolerance limit obtained by extending the ITU-T recommendation to 10Gb/s systems. At the high frequency end, the equipment could not generate a jitter large enough to measure the jitter tolerance. The open circle shows the largest jitter generated by the equipment and therefore the jitter tolerance is at least larger than that of open circle.

The jitter transfer function is specified with 3dB bandwidth and the peak value. The measured transfer function in Fig. 5 shows no peak value and the 3dB bandwidth of 6 MHz. The transfer function also satisfies the requirement extended from the ITU-T recommendation for 2.5Gb/s system. The rms jitter of the clock was measured by displaying the clock on the sampling scope with the trigger source from the reference clock of the pulse pattern generator. The rms jitter shown in Fig.6 is 1.7ps which is larger than 1ps recommended by ITU-T. This measurement, however, is not accurate due to the internal jitter of the sampling scope. An appropriate band-pass filter is also required in this measurement to reject the effect of the jitter both at a low frequency region including dc and at a high frequency region. The rms jitter estimated from the power spectrum of the extracted clock in Fig. 7 is 0.9ps. The decision phase margin was measured to be 60ps.

This CEDAR was adopted for the 10Gb/s transmission through an normal single-mode fiber with the length of 400km and the chromatic dispersion of ~17ps/nm km. The receiver sensitivity at the input of the optical preamplifier was -26.5dBm with the optical SNR of 24dB.

One of the important issues in CEDAR is to obtain a stable phase relationship between the incoming data and the extracted clock over the wide operating temperature. In this work this relative phase variation was minimized by adjusting the clock phase with the phase shifter whose control voltage is designed to vary according to the temperature utilizing a simple temperature sensor. The CEDAR compensated against the temperature in this fashion was tested for the temperature from -10 °C to 60 °C and showed no error in the whole temperature range. We, however, consider that the best method is to form a closed-loop control for the clock phase by using the decision circuit itself as the phase detector generating an appropriate feedback signal for the temperature compensation. The result of this work will also be presented.

CONCLUSION

We reported a PLL clock-extraction and data-regeneration circuit for 10Gb/s optical transmission system. The CEDAR was tested for the jitter characteristics and phase margin, and the test results satisfied the recommendation of ITU-T. The CEDAR compensated against the operating temperature through the automatic adjustment of the clock phase was tested for the

temperature from -10 °C to 60 °C and showed no error during the whole measurement period.

ACKNOWLEDGMENTS

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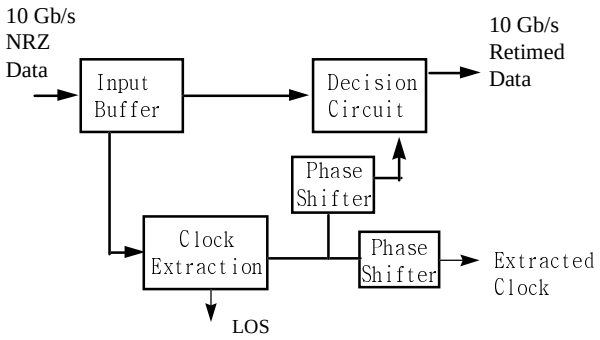

Fig. 1 The block diagram of 10Gb/s clock-extraction and data-regenerator circuit

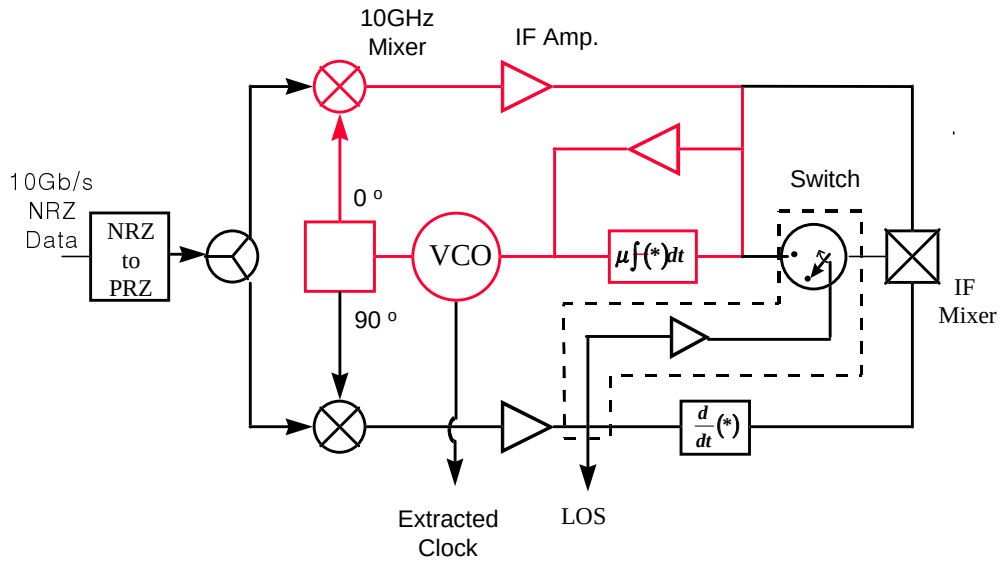

Fig. 2 The block diagram of the clock extraction circuit

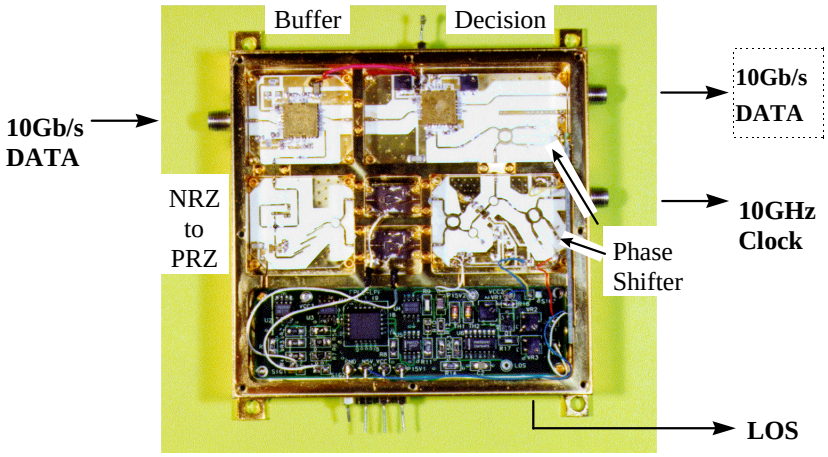

Fig. 3 The photograph of the 10Gb/s CEDAR module

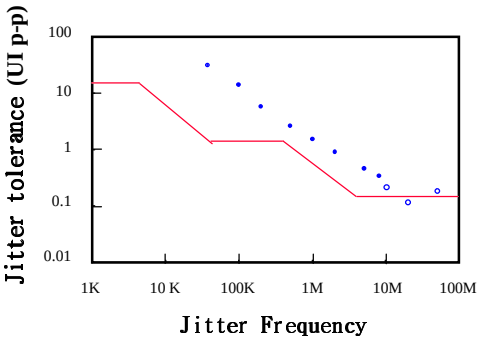

Fig. 4 The measured jitter tolerance: solid line = jitter tolerance specifications, • = the measured jitter tolerance, o < the jitter tolerance.

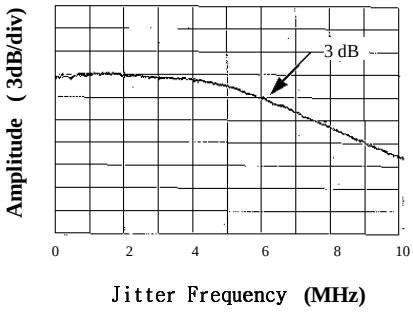

Fig. 5 The jitter transfer function of the 10Gb/s CEDAR

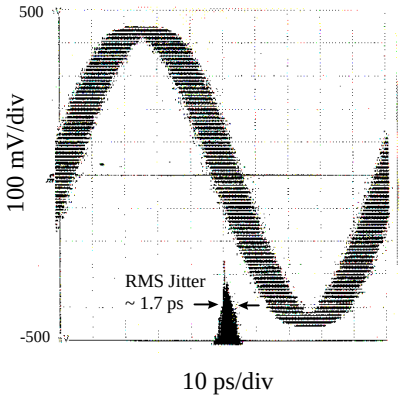

Fig. 6 The 10GHz extracted clock waveform

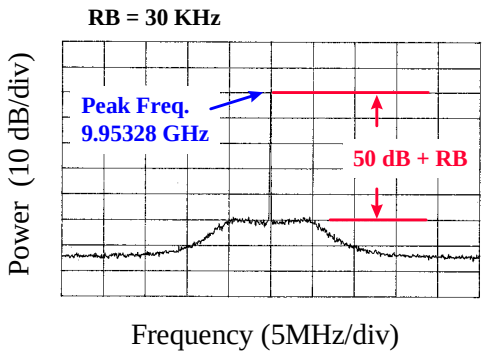

Fig. 7 The power spectrum of the extracted clock.